# TJA1057

## High-speed CAN transceiver

Rev. 2 — 30 October 2013 Product data sheet

## 1. General description

The TJA1057 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1057 offers a feature set optimized for 12 V automotive applications, with significant improvements over NXP's first- and second-generation CAN transceivers, such as the TJA1050, and excellent ElectroMagnetic Compatibility (EMC) performance. The TJA1057 also displays ideal passive behavior to the CAN bus when the supply voltage is off.

These features make the TJA1057 an excellent choice for HS-CAN networks that only require basic CAN functionality. The TJA1057GT variant guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbps as used in, for example, CAN FD networks.

## 2. Features and benefits

### 2.1 General

- Fully ISO 11898-2 compliant
- Optimized for use in 12 V automotive systems
- Excellent ElectroMagnetic Compatibility (EMC) performance, satisfying 'Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications', Version 1.3, May 2012.
- Compatible with 5 V and 3V3 microcontrollers

### 2.2 Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions
- Transceiver disengages from bus when not powered (zero load) or in Silent mode
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pin $V_{CC}$
- Internal biasing of TXD and S input pins

### 2.3 Protection

- High ESD handling capability on the bus pins (6 kV IEC and HBM)
- Bus pins protected against transients in automotive environments

- Thermally protected

### 2.4 TJA1057GT

- Loop delay symmetry guaranteed for data rates up to 5 Mbps
- Improved TXD to RXD propagation delay of 210 ns

## 3. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 4.75 | - | 5.25 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | 3.5 | 4 | 4.3 | V |
| $I_{CC}$ | supply current | Silent mode | 100 | - | 800 | μA |
| | | Normal mode; bus recessive | 2 | 5 | 10 | mA |
| | | Normal mode; bus dominant | 20 | 45 | 70 | mA |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 at pins CANH and CANL | –6 | - | +6 | kV |
| $V_{CANH}$ | voltage on pin CANH | no time limit; DC limiting value | –42 | - | +42 | V |
| $V_{CANL}$ | voltage on pin CANL | no time limit; DC limiting value | –42 | - | +42 | V |
| $T_{vj}$ | virtual junction temperature | | –40 | - | +150 | °C |

## 4. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TJA1057T | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| TJA1057GT | | | |

## 5. Block diagram

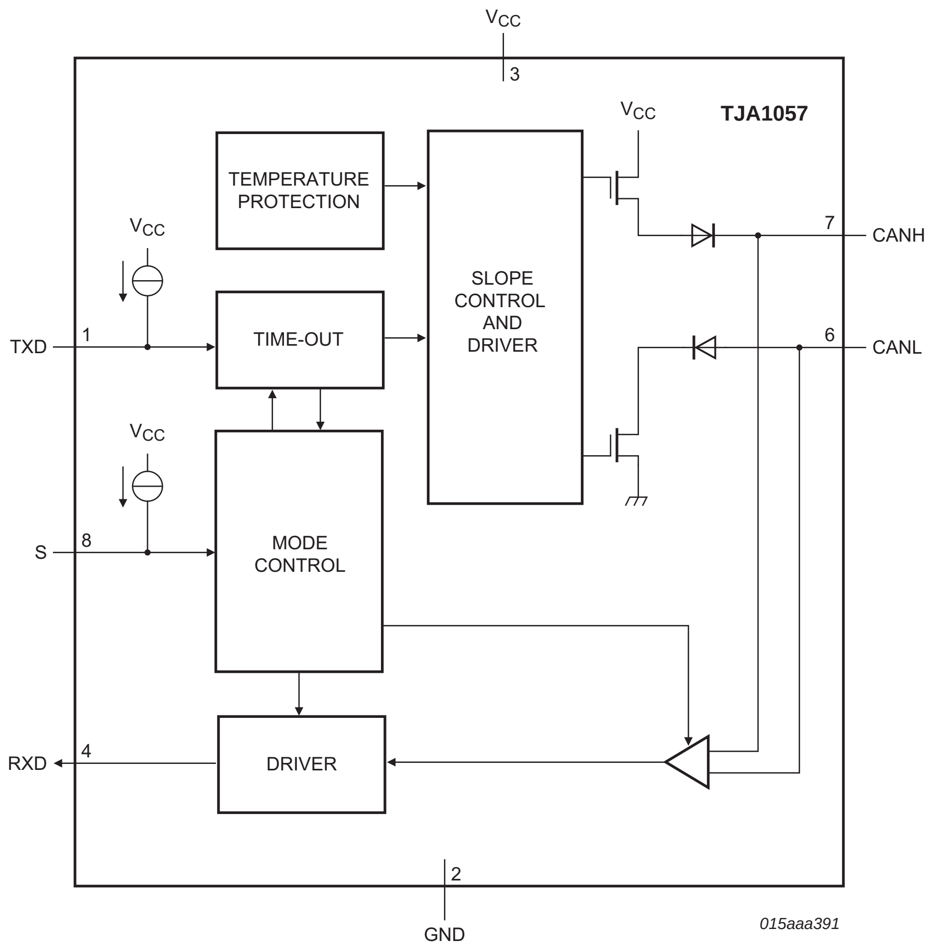



**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

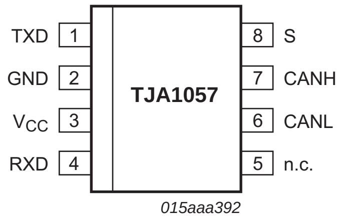



**Fig 2. Pin configuration diagram**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| TXD | 1 | transmit data input |
| GND | 2 | ground |
| $V_{CC}$ | 3 | supply voltage |
| RXD | 4 | receive data output; reads out data from the bus lines |
| n.c. | 5 | not connected |
| CANL | 6 | LOW-level CAN bus line |
| CANH | 7 | HIGH-level CAN bus line |
| S | 8 | Silent mode control input |

# 7. Functional description

## 7.1 Operating modes

The TJA1057 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

**Table 4. Operating modes**

| Mode | Inputs | | Outputs | |
|---|---|---|---|---|
| | Pin S | Pin TXD | CAN driver | Pin RXD |
| Normal | LOW | LOW | dominant | LOW |
| | | HIGH | recessive | LOW when bus dominant |
| | | | | HIGH when bus recessive |
| Silent | HIGH | x[1] | biased to recessive | follows bus |

[1] 'x' = don't care.

### 7.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines, CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible EME.

### 7.1.2 Silent mode

A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting all network communications.

## 7.2 Fail-safe features

### 7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

### 7.2.2 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to $V_{CC}$ to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Silent mode to minimize standby current.

### 7.2.3 Undervoltage detection on pins $V_{CC}$

If $V_{CC}$ drops below the undervoltage detection level, $V_{uvd(VCC)}$, the transceiver switches off.

### 7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers recover once TXD has been reset to HIGH. Including the TXD condition prevents output driver oscillation due to small variations in temperature.

## 8. Limiting values

**Table 5. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_x$ | voltage on pin x | DC value | | | | |
| | | on pins CANH, CANL | | –42 | +42 | V |
| | | on pin $V_{CC}$ | | –0.3 | +6 | V |
| | | on any other pin | [1] | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{trt}$ | transient voltage | on pins CANH and CANL | [2] | –150 | +100 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 | [3] | | | |
| | | at pins CANH and CANL | [4] | –6 | +6 | kV |
| | | HBM | [5] | | | |
| | | at pins CANH and CANL | | –6 | +6 | kV |
| | | at any other pin | | –4 | +4 | kV |
| | | MM | [6] | | | |
| | | at any pin | | –200 | +200 | V |
| | | CDM | [7] | | | |
| | | at corner pins | | –750 | +750 | V |
| | | at any pin | | –500 | +500 | V |
| $T_{vj}$ | virtual junction temperature | | [8] | –40 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |

[1] No time limit.

[2] Verified by IBEE Zwickau to ensure that pins CANH and CANL can withstand ISO 7637 part 3 automotive transient test pulses 1, 2a, 3a and 3b.

[3] IEC 61000-4-2 (150 pF, 330 Ω); direct coupling.

[4] ESD performance of pins CANH and CANL according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house. The result is equal to or better than ±6 kV (unaided).

[5] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[6] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[7] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF); grade C3B.

[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of $T_{vj}$. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).

## 9. Thermal characteristics

**Table 6. Thermal characteristics**
*According to IEC 60747-1.*

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | thermal resistance from virtual junction to ambient | SO8 package; in free air | 97 | K/W |

## 10. Static characteristics

**Table 7. Static characteristics**

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.*[1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply; pin $V_{CC}$** | | | | | | | |
| $V_{CC}$ | supply voltage | | | 4.75 | - | 5.25 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | | 3.5 | 4 | 4.3 | V |
| $I_{CC}$ | supply current | Silent mode; $V_{TXD} = V_{CC}$ | | 0.1 | - | 2.5 | mA |
| | | Normal mode | | | | | |
| | | recessive; $V_{TXD} = V_{CC}$ | | 2 | 5 | 10 | mA |
| | | dominant; $V_{TXD}$ = 0 V | | 20 | 45 | 70 | mA |
| **Silent mode control input; pin S** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | 2 | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | | −0.3 | - | 0.8 | V |
| $I_{IH}$ | HIGH-level input current | $V_S = V_{CC}$ | | −1 | - | +1 | μA |
| $I_{IL}$ | LOW-level input current | $V_S$ = 0 V | | −15 | - | −1 | μA |
| **CAN transmit data input; pin TXD** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | 2 | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | | −0.3 | - | 0.8 | V |
| $I_{IH}$ | HIGH-level input current | $V_{TXD} = V_{CC}$ | | −5 | - | +5 | μA |
| $I_{IL}$ | LOW-level input current | $V_{TXD}$ = 0 V | | −260 | −150 | −70 | μA |
| $C_i$ | input capacitance | | [2] | - | 5 | 10 | pF |
| **CAN receive data output; pin RXD** | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{RXD} = V_{CC}$ − 0.4 V | | −8 | −3 | −1 | mA |
| $I_{OL}$ | LOW-level output current | $V_{RXD}$ = 0.4 V; bus dominant | | 1 | - | 12 | mA |
| **Bus lines; pins CANH and CANL** | | | | | | | |
| $V_{O(dom)}$ | dominant output voltage | $V_{TXD}$ = 0 V; $t < t_{to(dom)TXD}$ | | | | | |
| | | pin CANH | | 2.75 | 3.5 | 4.5 | V |
| | | pin CANL | | 0.5 | 1.5 | 2.25 | V |
| $V_{dom(TX)sym}$ | transmitter dominant voltage symmetry | $V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$ | | −400 | - | +400 | mV |
| $V_{O(dif)bus}$ | bus differential output voltage | $V_{TXD}$ = 0 V; $t < t_{to(dom)TXD}$<br>$R_L$ = 50 Ω to 65 Ω | | 1.5 | - | 3 | V |
| | | $V_{TXD} = V_{CC}$; bus recessive; no load | | −50 | - | +50 | mV |
| $V_{O(rec)}$ | recessive output voltage | $V_{TXD} = V_{CC}$; no load | | 2 | $0.5V_{CC}$ | 3 | V |
| $V_{th(RX)dif}$ | differential receiver threshold voltage | $V_{cm(CAN)}$ = −12 V to +12 V; Normal/Silent mode | [3] | 0.5 | - | 0.9 | V |
| $V_{hys(RX)dif}$ | differential receiver hysteresis voltage | $V_{cm(CAN)}$ = −12 V to +12 V Normal mode | | 50 | - | 300 | mV |
| $I_{O(dom)}$ | dominant output current | $V_{TXD}$ = 0 V; $t < t_{to(dom)TXD}$; $V_{CC}$ = 5 V | | | | | |
| | | pin CANH; $V_{CANH}$ = 0 V | | −100 | −70 | −40 | mA |
| | | pin CANL; $V_{CANL}$ = 5 V / 40 V | | 40 | 70 | 100 | mA |

**Table 7. Static characteristics** *…continued*

*$T_{vj}$ = –40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.*[1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{O(rec)}$ | recessive output current | Normal mode; $V_{TXD}$ = $V_{CC}$ $V_{CANH}$ = $V_{CANL}$ = –27 V to +32 V | | –5 | - | +5 | mA |
| $I_L$ | leakage current | $V_{CC}$ = 0 V; $V_{CANH}$ = $V_{CANL}$ = 5 V | | –5 | - | +5 | μA |
| $R_i$ | input resistance | | | 9 | 15 | 28 | kΩ |
| $\Delta R_i$ | input resistance deviation | between $V_{CANH}$ and $V_{CANL}$ | | –3 | - | +3 | % |
| $R_{i(dif)}$ | differential input resistance | | | 19 | 30 | 52 | kΩ |
| $C_{i(cm)}$ | common-mode input capacitance | | [2] | - | - | 20 | pF |
| $C_{i(dif)}$ | differential input capacitance | | [2] | - | - | 10 | pF |
| **Temperature detection** | | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | | [2] | - | 185 | - | °C |

[1] Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Guaranteed by design.

[3] $V_{cm(CAN)}$ is the common mode voltage of CANH and CANL.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**
*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.75 V to 5.25 V; $R_L$ = 60 Ω; $C_L$ = 100 pF unless specified otherwise. All voltages are defined with respect to ground.*[1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3 and Figure 4** | | | | | | | |
| $t_{d(TXD-busdom)}$ | delay time from TXD to bus dominant | Normal mode | | - | 65 | - | ns |
| $t_{d(TXD-busrec)}$ | delay time from TXD to bus recessive | Normal mode | | - | 90 | - | ns |
| $t_{d(busdom-RXD)}$ | delay time from bus dominant to RXD | Normal mode | | - | 60 | - | ns |
| $t_{d(busrec-RXD)}$ | delay time from bus recessive to RXD | Normal mode | | - | 65 | - | ns |
| $t_{PD(TXD-RXD)}$ | propagation delay from TXD to RXD | TJA1057T; Normal mode | | 50 | - | 230 | ns |
| | | TJA1057GT; Normal mode | | 50 | - | 210 | ns |
| | | TJA1057GT; Normal mode; $R_L$ = 120 Ω; $C_L$ = 200 pF | [2] | - | - | 300 | ns |
| $t_{bit(RXD)}$ | bit time on pin RXD | TJA1057GT only; $t_{bit(TXD)}$ = 500 ns | [3] | 400 | - | 550 | ns |
| | | TJA1057GT only; $t_{bit(TXD)}$ = 200 ns | [3] | 120 | - | 220 | ns |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | $V_{TXD}$ = 0 V; Normal mode | | 0.8 | 3 | 16 | ms |

[1] Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Guaranteed by design.

[3] See Figure 5.

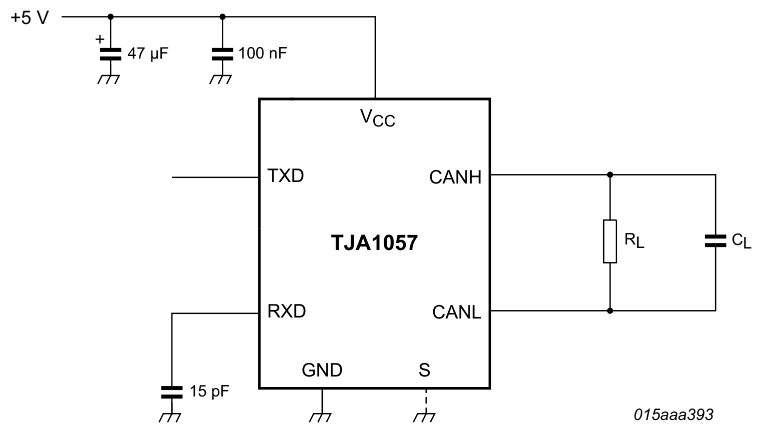



**Fig 3. CAN transceiver timing test circuit**

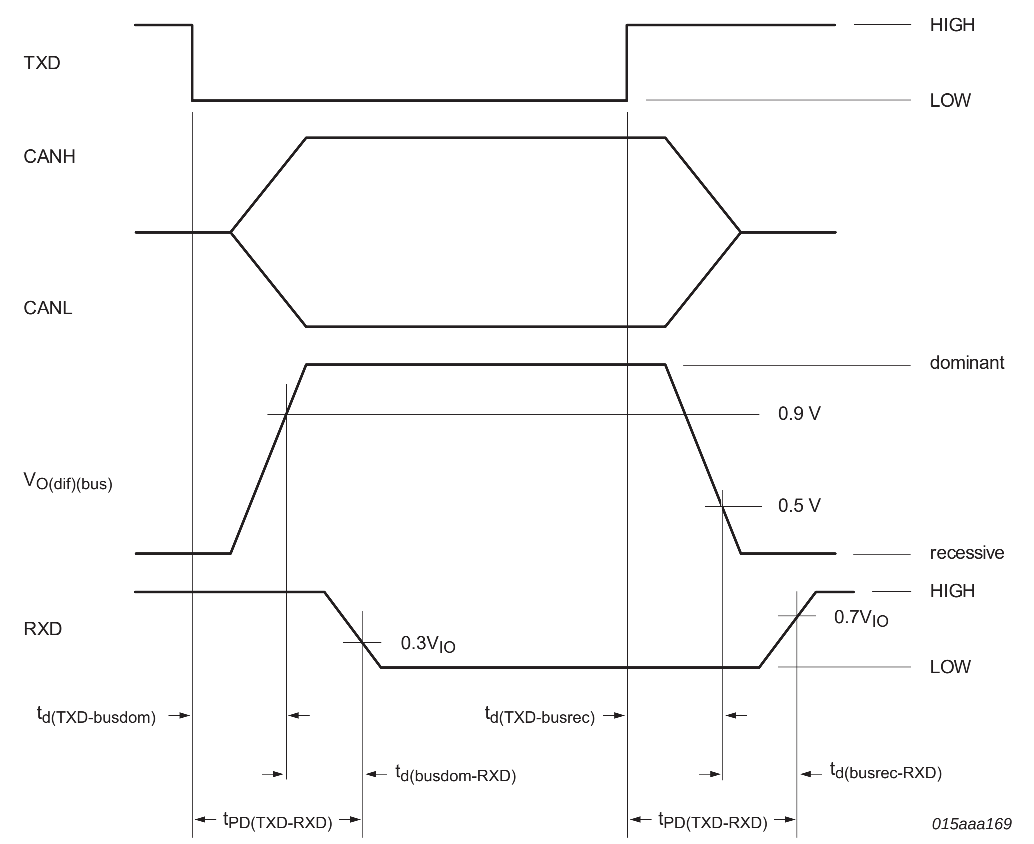



**Fig 4. CAN transceiver timing diagram**

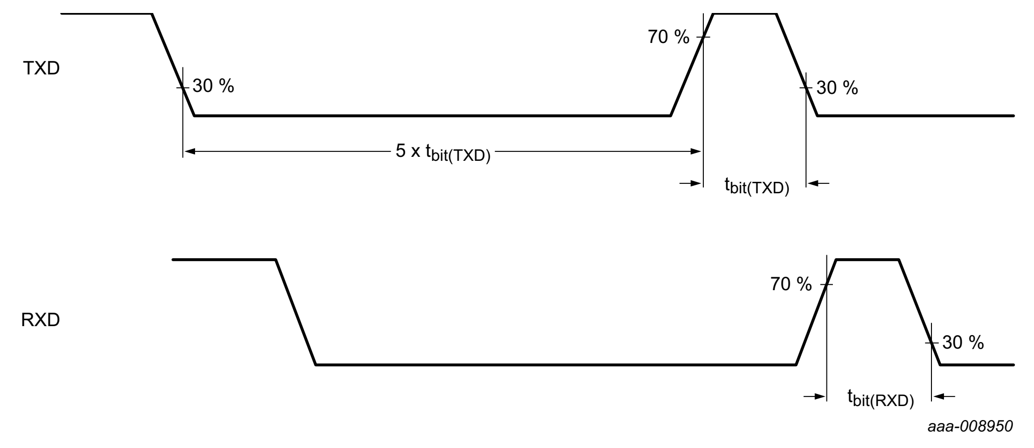



**Fig 5. Loop delay symmetry timing diagram (TJA1057GT only)**

# 12. Application information

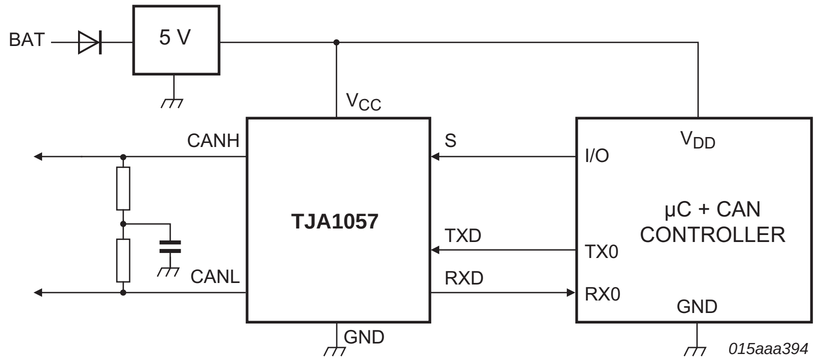



**Fig 6. Typical TJA1057 application with a 5 V microcontroller.**

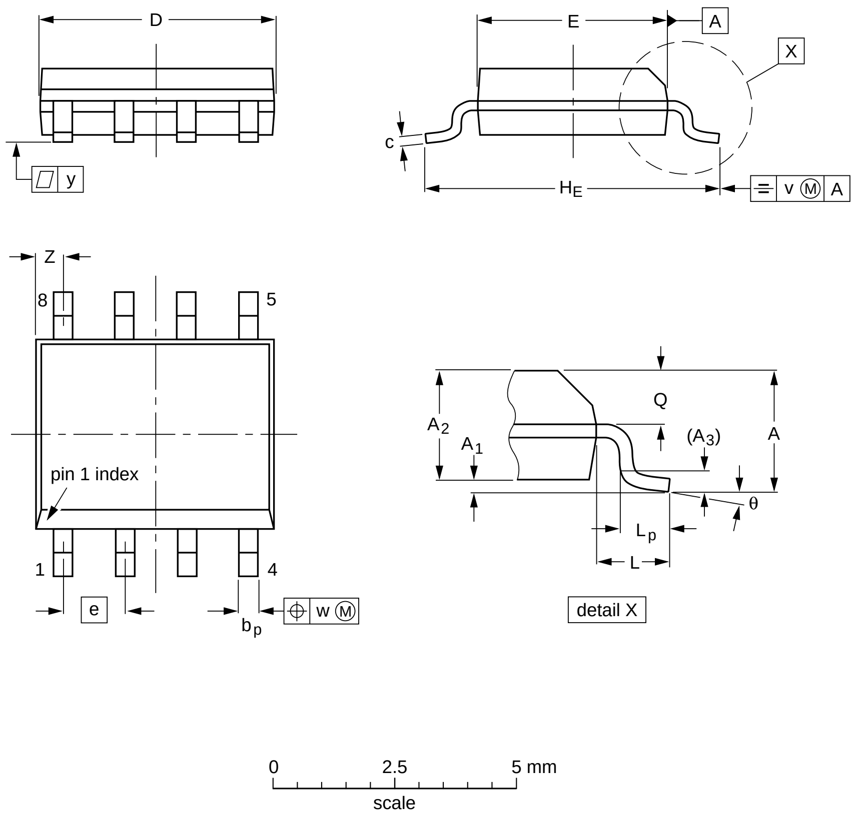
# 13. Test information

## 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

## 14. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 7. Package outline SOT96-1 (SO8)**

## 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

**Table 9. SnPb eutectic process (from J-STD-020D)**

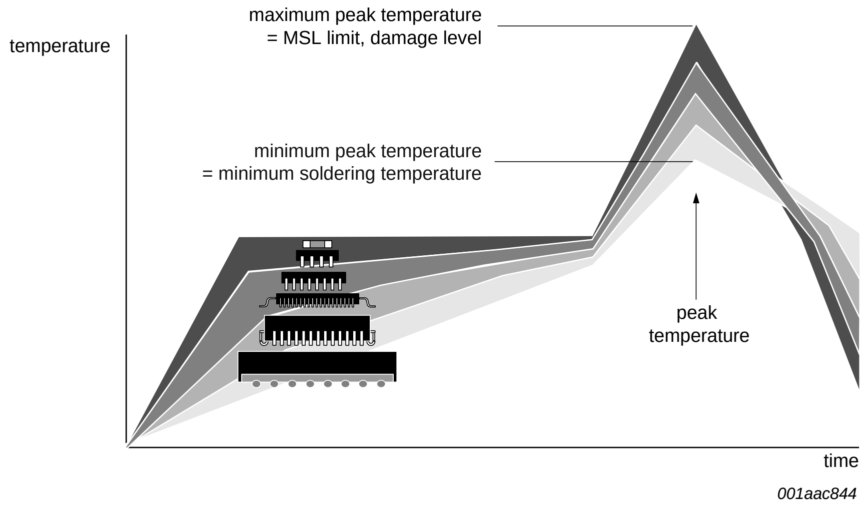
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 10. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.




MSL: Moisture Sensitivity Level

**Fig 8. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJA1057 v.2 | 20131030 | Product data sheet | - | TJA1057 v.1 |
| Modifications: | • specification status changed to 'Product'<br>• added Mantis logo on front page<br>• added TJA1057GT variant:<br>– Section 1, Table 2: text amended<br>– Section 2.4: added<br>– Table 8: parameter $t_{PD(TXD-RXD)}$ amended; parameter $t_{bit(RXD)}$ added<br>– Figure 5: added<br>• Section 2.1: text amended<br>• Table 5, Table note 2: text amended<br>• Table 7, table header text amended ($C_L$ added); Table note 1, Table note 2 text amended<br>• Table 8, table header text amended ($C_L$ added, last sentence deleted); Table note 1 text amended; parameter value added: $t_{PD(TXD-RXD)}$ along with associated table note (Table note 2)<br>• Figure 3 amended | | | |
| TJA1057 v.1 | 20130530 | Preliminary data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 18.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 18.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications —** This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Quick reference data —** The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Translations —** A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 20. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 30 October 2013**

**Document identifier: TJA1057**